Syllabus & Scheme for

M.Tech. (VLSI Design)

Department of Electronics Engineering
YMCA University of Science & Technology,
Faridabad (Haryana)
Total credit requirement of the course : 71  Max. Marks: 2250
Core Courses : 10  Labs : 06
Electives Courses : 02  Seminar : 01
Project / Dissertation : 02

**First Semester**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Title</th>
<th>Credit (L-T-P)</th>
<th>Marks Weightage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Theory</td>
</tr>
<tr>
<td>E 601 V</td>
<td>Physics of Semiconductor Devices</td>
<td>4 4-0-0</td>
<td>60</td>
</tr>
<tr>
<td>E 603 V</td>
<td>Digital VLSI Design</td>
<td>4 4-0-0</td>
<td>60</td>
</tr>
<tr>
<td>E 605 V</td>
<td>Hardware Description Language for VLSI</td>
<td>4 4-0-0</td>
<td>60</td>
</tr>
<tr>
<td>E 607 V</td>
<td>Embedded System Design I</td>
<td>4 4-0-0</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Sessional</td>
</tr>
<tr>
<td>E 609 V</td>
<td>Embedded System Lab-I</td>
<td>1 0-0-2</td>
<td>20</td>
</tr>
<tr>
<td>E 611 V</td>
<td>Digital VLSI Design Lab</td>
<td>1 0-0-2</td>
<td>20</td>
</tr>
<tr>
<td>E 613 V</td>
<td>HDL Lab</td>
<td>1 0-0-2</td>
<td>20</td>
</tr>
</tbody>
</table>

|              |                                                 |                | External | Internal|
|              |                                                 |                |          |         |
| Total        | 19                                              | 16-0-6         | 300      | 250     |

Instruction:
1. Sessional will be awarded by the teacher in marks only.
2. Theory paper will be awarded in marks.
3. Combining the theory and sessional marks university will compute percentage of marks in that subject.
4. On the basis of combined percentage of marks in a particular paper, the grade will be allocated according to the minutes of the BOS meeting held on 22/05/2010.
## Second Semester

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Title</th>
<th>Credit (L-T-P)</th>
<th>Marks Weightage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Theory</td>
</tr>
<tr>
<td>E 602 V</td>
<td>Analog VLSI Design</td>
<td>4 4-0-0</td>
<td>60</td>
</tr>
<tr>
<td>E 604 V</td>
<td>IC Fabrication Technology</td>
<td>4 4-0-0</td>
<td>60</td>
</tr>
<tr>
<td>E 606 V</td>
<td>Embedded System Design-II</td>
<td>4 4-0-0</td>
<td>60</td>
</tr>
<tr>
<td>E 608 V</td>
<td>ASICs and FPGAs</td>
<td>4 4-0-0</td>
<td>60</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Title</th>
<th>Credit (L-T-P)</th>
<th>Marks Weightage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>External</td>
</tr>
<tr>
<td>E 610 V</td>
<td>Analog VLSI Lab</td>
<td>1 0-0-2</td>
<td>20</td>
</tr>
<tr>
<td>E 612 V</td>
<td>Embedded System Lab -II</td>
<td>1 0-0-2</td>
<td>20</td>
</tr>
<tr>
<td>E 614 V</td>
<td>Seminar</td>
<td>1 0-0-2</td>
<td>--</td>
</tr>
</tbody>
</table>

Total: 19 16-0-6 280 270

**Instruction:**
1. Sessional will be awarded by the teacher in marks only.
2. Theory paper will be awarded in marks.
3. Combining the theory and sessional marks university will compute percentage of marks in that subject.
4. On the basis of combined percentage of marks in a particular paper, the grade will be allocated according to the minutes of the BOS meeting held on 22/05/2010.
### Third Semester

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Title</th>
<th>Credit (L-T-P)</th>
<th>Marks Weightage</th>
<th>Theory</th>
<th>Sessional</th>
</tr>
</thead>
<tbody>
<tr>
<td>E 701 V</td>
<td>Advanced Digital Signal Processing</td>
<td>4 4-0-0</td>
<td>60</td>
<td></td>
<td>40</td>
</tr>
<tr>
<td>E 703 V</td>
<td>Nanotechnology</td>
<td>4 4-0-0</td>
<td>60</td>
<td></td>
<td>40</td>
</tr>
<tr>
<td>E 705 V</td>
<td>Elective-I</td>
<td>4 4-0-0</td>
<td>60</td>
<td></td>
<td>40</td>
</tr>
<tr>
<td>E 707 V</td>
<td>Elective-II</td>
<td>4 4-0-0</td>
<td>60</td>
<td></td>
<td>40</td>
</tr>
<tr>
<td>E 709 V</td>
<td>Minor Project</td>
<td>4 0-0-4</td>
<td>80</td>
<td></td>
<td>120</td>
</tr>
<tr>
<td>E 711 V</td>
<td>ADSP lab</td>
<td>1 0-0-2</td>
<td>20</td>
<td></td>
<td>30</td>
</tr>
</tbody>
</table>

**Total** 21 16-0-10 340 310

### Fourth Semester

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Title</th>
<th>Credit (L-T-P)</th>
<th>Marks Weightage</th>
<th>Theory</th>
<th>Sessional</th>
</tr>
</thead>
<tbody>
<tr>
<td>E 702 V</td>
<td>Dissertation</td>
<td>12 0-0-24</td>
<td>200</td>
<td></td>
<td>300</td>
</tr>
</tbody>
</table>

**Total** 12 0-0-24 200 300

**Instruction:**
1. Sessional will be awarded by the teacher in marks only.
2. Theory paper will be awarded in marks.
3. Combining the theory and sessional marks university will compute percentage of marks in that subject.
4. On the basis of combined percentage of marks in a particular paper, the grade will be allocated according to the minutes of the BOS meeting held on 22/05/2010.
Elective - I

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Subject Code</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>E 705(A) V</td>
<td>VLSI Architecture</td>
</tr>
<tr>
<td>2</td>
<td>E 705(B) V</td>
<td>Embedded Control System</td>
</tr>
<tr>
<td>3</td>
<td>E 705(C) V</td>
<td>Mixed signal Embedded System</td>
</tr>
<tr>
<td>4</td>
<td>E 705(D) V</td>
<td>CAD system Environment</td>
</tr>
</tbody>
</table>

Elective – II

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Subject Code</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>E 707(A) V</td>
<td>VLSI Testing and Design for Testability</td>
</tr>
<tr>
<td>2.</td>
<td>E 707(B) V</td>
<td>Low Power VLSI design</td>
</tr>
<tr>
<td>3</td>
<td>E 707(C) V</td>
<td>CAD for VLSI</td>
</tr>
<tr>
<td>4</td>
<td>E 707(D) V</td>
<td>Algorithm for VLSI Design Automation</td>
</tr>
</tbody>
</table>
**Semester I**

**Physics of Semiconductor Devices**

Semiconductor Electronics: Physics of Semiconductor Materials, Drift Velocity, Mobility, Scattering, Diffusion current, Band Model.

Metal Semiconductor Contacts: Metal-Semiconductor System, (V-I) and (C-V) equations for a Shottky - Barrier - Diode, Diode Construction, Device analysis using surface - states, applications as mixer and detectors in microwave region, Ohmic Contacts, Surface effects.

PN Junctions: Step junction, Linearly Graded Junction, (V-I) and (C-V) characteristics, Junction Breakdown, tunneling effect, avalanche multiplication, transient behaviour and noise. Use of junction diode as a rectifier, Voltage regulator, resistor varactor and fast recovery diode.

Bipolar Junction Transistors: Transistor action, Current -Voltage equation, output characteristics, breakdown voltage, Ebers-Moll and Gummel - Poon Model, early effect, Charge control model, small-signal transistor model, Simulation model,


MOS Transistors: Basic Theory, structure and operation, MOSFET parameters, Threshold Voltage and its control, Geometric effects on threshold, Ion-Implanted MOSFETs, Complementary MOSFET, Sub-threshold Conduction, velocity saturation, hot carriers, small geometry considerations

**TEXT BOOKS:**


**REFERENCE BOOKS:**

UNIT I REVIEW OF MOS TECHNOLOGY
Evolution of VLSI technology, VLSI Design Flow, Basic MOS Transistor: Enhancement and depletion mode, MOS structure, NMOS, PMOS and CMOS fabrication.

UNIT II ELECTRICAL PROPERTIES OF MOS
Threshold voltage, MOSFET current voltage characteristics, second order effects, MOS inverters: VTC characteristics of NMOS inverter, CMOS inverter and Bi-CMOS inverter. Noise margins, Latch-up in CMOS circuits.

UNIT III DESIGN PROCESS
Physical design of simple and complex logic gates using NMOS and CMOS technology, Stick diagrams, NMOS Design Style, CMOS Design Style, Lambda based Design Rules. Layout.

UNIT IV MOS TRANSISTOR SWITCHING CHARACTERISTICS
Sheet resistance, area capacitance, inverter delay. Switching power dissipation of CMOS inverters.

UNIT V DYNAMIC LOGIC CIRCUITS
CMOS Logic Structure: Complementary CMOS Logic, Pseudo NMOS Logic, Dynamic CMOS Logic, CMOS Domino Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS transmission gate Logic

UNIT VI SCALING OF MOS CIRCUITS
Scaling models, scaling factor for device parameters, Advantages and Limitations of scaling.

UNIT VII SUBSYSTEM DESIGN
Architectural issues in VLSI, Design of CMOS parity generator, Multiplexer, n-Bit Comparator, Incrementer/Decrementer, ALU subsystem.

TEXT BOOKS:
3. Introduction to Digital Circuits: Rabaey (PH)
Hardware Description Languages for VLSI


VHDL Background: VHDL History, Existing Languages, VHDL Requirements, The VHDL Language.

Design Methodology Based On VHDL: Elements of VHDL, Top down Design, Top down Design with VHDL, Subprograms, VHDL Operators, Conventions and Syntax.

Basic Concepts In VHDL: Characterizing Hardware Languages, Objects and Classes, Signal Assignments, Concurrent and Sequential Assignments.


Utilities For High-Level Descriptions: Type Declarations, VHDL Operators, Subprogram Parameter Types and Overloading, Predefined Attributes, User Defined Attributes.


Verilog: Overview of Digital design with Verilog HDL, basic concepts, modules & ports.

TEXT BOOKS:

REFERENCE BOOKS:
Embedded System-I

MICROCONTROLLER 8051

Introduction, 8051 architecture and programming model. Internal RAM and registers, I/O ports, Interrupt system

PROGRAMMING WITH 8051


PERIPHERALS & INTERFACING

Timers and counters Serial Communications, Interrupts programming, Interfacing LCD, ADC and sensors, Interfacing stepper motors, keyboards and DAC’S. Interfacing external memory and 8255

MOTOROLA 68HC11 MICROCONTROLLER


REAL TIME OPERATING SYSTEM

Real time operating system overview, Exposure to Windows CE, QNX, Micro kernels and pc/US of introduction to process models. Interrupt routines in an RTOS environment. Encapsulation semaphores and queues, hard real-time scheduling considerations, saving memory space.

Books :

Semester II

Analog VLSI Design

Small Signal & large signal Models of MOS & BJT transistor. Analog MOS Process

MOS & BJT Transistor Amplifiers: Single transistor Amplifiers stages: Common Emitter, Common base, Common Collector, Common Drain, Common Gate & Common Source Amplifiers


Current Mirrors, Active Loads & References
Current Mirrors: Simple current mirror, Cascode current mirrors, Widlar current mirror, Wilson Current mirror, etc. Active loads, Voltage & current references. Analysis of Differential Amplifier with active load, supply and temperature independent biasing techniques, Frequency Response.

Operational Amplifier: Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascodes, MOS telescopic-cascode operational amplifiers, MOS Folded-cascode operational amplifiers, Frequency response & compensation.

Nonlinear Analog Circuits:
Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters, Voltage controlled oscillator, Comparators, Phase Locked Loops (PLL)

OTA & Switched Capacitor filters
OTA Amplifiers. Switched Capacitor Circuits and Switched Capacitor Filters.

Text:

References:
IC Fabrication Technology

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modelling and technology; Ion Implantation modelling, technology and damage annealing; characterisation of Impurity profiles.

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterisation of oxide films; High k and low k dielectrics for ULSI.

Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

Chemical Vapour Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modelling and technology.

Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallisation schemes.

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.

Recent Trends in Fabrication, Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology.

Texts/References:
ASICs and FPGAs

Introduction: course outline, logistics introduction to ASICs, FPGAs, economics

HDL: Logic design Review, Behavior, dataflow, structural modeling, control statements, FSM modeling

CMOS Review: Classical, CMOS (Deep Sub-micron), ASIC Methodologies

Fabrication of MOSFET: MOS Transistor, Design methodologies, design for testability.

FPGA: Programmable logic FPGA, Configuration logic blocks, Function Generator, ROM implementation, RAM implementation, time skew buffers, FPGA Design tools, Network-on-chip, Adaptive System-on-chip, AES ASIC Implementation, Advanced FPGA Design

Logic synthesis: Fundamentals, logic synthesis with synopsis, physical design compilation, simulation, implementation. V Floor planning and placement, Commercial EDA tools for synthesis.

Testing: Advanced interconnects and testing techniques

Text / Reference Books:
Embedded System Design-II

THE PIC MICROCONTROLLER ARCHITECTURE

CPU, ALU, Data Movement, The Program Counter and Stack, Reset, Interrupts, Architecture Differences, Mid-Range instruction Set

PIC HARDWARE FEATURES

Power Input and Decoupling, Reset, Watchdog Timer, System Clock/Oscillators, Configuration Registers, Sleep, Hardware and File Registers, Parallel Input Output, Interrupts, Prescaler, The OPTION Register, Mid-Range Built-In EEPROM Flash Access, TMR1 and TMR2 Serial I/O, Analog I/O, Parallel Slave Port (PSP), External Memory Connections, In-Circuit Serial Programming (ISCP)

PROGRAMMING WITH PIC

Assembly Language Programming, Hex File Format, Code-Protect Features, Programming, PIC Emulators

HARDWARE INTERFACING

Estimating Application Power Requirements, Reset, Interfacing to External Devices, LEDs, Switch Bounce, Matrix Keypads, LCDs, Analog I/O, Relays and Solenoids, DC and Stepper Motors, Servo Control Serial Interfaces

ARM PROCESSOR FUNDAMENTALS

Registers, State and Instruction Sets, Pipeline, Memory Management, Introduction to the ARM Instruction Set

Books

**Semester III**

**Advanced Digital Signal Processing**


2. **Fourier Transform & inverse Fourier transform**: Frequency domain design of digital filters, Fourier transform, use of Fourier transform in Signal processing. The inverse fourier transform, Sampling continuous function to generate a sequence, Reconstruction of continuous -time signals from Discrete-time sequences.

3. **DFT & FFT & Z transform with Applications**: Discrete Fourier transform, properties of DFT, Circular Convolution, Fast Fourier Transform, Realizations of OFT. The Ztransform, the system function of a digital filter, Digital Filter implementation from the system function, the inverse Z- transform, properties & applications, Special computation of finite sequences, sequence of infinite length & continuous time signals, computation of fourier series & time sequences from spectra.

4. **Digital Filter Structure & Implementation**: Linearity, time- invariance & causality, the discrete convolution, the transfer function, stability tests, steady state response, Amplitude & Phase characteristics, stabilization procedure, Ideal LP Filter. Physical reliability & specifications.FIR Filters, Truncation windowing & Delays, design example, IIR Filters: Review of design of analog filters & analog frequency transformation. Digital frequency transformation. Design of LP filters using impulse invariance method, Bilinear transformation, Phase equalizer, digital all pass filters.

5. **Implementation of Filters**: Realization block diagrams, Cascade & parallel realization, effect of infinite-word length, transfer function of degree 1&2, Sensitivity comparisons, effects of finite precision arithmetic on Digital filters.

**TextBooks**
1. Alam V. Oppenheim & Ronald W. Schafer, "Digital Signal Processing" PHI.

**Reference Books**
Nanotechnology

Unit - I Atomic structure
Basic crystallography, Crystals and their imperfections, Diffusion, Nucleation and crystallization, Metals, Semiconductors and Insulators, Phase transformations, Ceramic materials.

Unit – II Physical Properties of Materials
Electrical and Thermal properties, Optical properties of materials, Magnetic properties of materials, Density of states, Coulomb blockade, Kondo effect, Hall effect, Quantum Hall Effect.

Unit – III Nanostructures

Unit – IV Characterization of Nanomaterials

Reference Books:

1. Introduction to solid state Physics : C.Kittel
2. Introduction to theory of solids : H.M. Roenberg
3. Physics and Chemistry of materials : Joel I. Gersten
4. Handbook of Nanotechnology : Bharat Bhushan(spriniger)
Elective I

VLSI Architectures

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers.

Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

Advanced processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization, Scalable point –point interfaces: Alpha364 and HT protocols, high performance signaling layer.

Text:

1. Kai Hwang, “Advanced computer architecture”; TMH.

References:

1. J.P.Hayes, “computer Architecture and organization”; MGH.
2. Harvey G.Cragon, ”Memory System and Pipelined processors”; Narosa Publication.
3. V.Rajaranam & C.S.R.Murthy, “Parallel computer”; PHI.
Embedded Control System

INTRODUCTION
Controlling the hardware with software – Data lines, Address lines, Ports – Schematic representation – Bit masking – Programmable peripheral interface – Switch input detection – 74 LS 244

INPUT-OUTPUT DEVICES

D/A AND A/D CONVERSION
R 2R ladder - Resistor network analysis - Port offsets - Triangle waves analog vs. digital values - ADC0809 – Auto port detect - Recording and playing back voice - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.

ASYNCHRONOUS SERIAL COMMUNICATION

CASE STUDIES: EMBEDDED C PROGRAMMING
Multiple closure problems – Basic outputs with PPI – Controlling motors – Bi-directional control of motors – H bridge – Telephonic systems – Stepper control – Inventory control systems.

TEXT BOOKS:

REFERENCE BOOKS:
Mixed Signal Embedded System

INTRODUCTION TO SYSTEM DESIGN

Dynamic Range, Calibration, Bandwidth, Processor Throughput, Avoiding Excess Speed, Other System Considerations, Sample Rate and Aliasing

DAC & ADC
Introduction - Nyquist rate converters – Over sampling converters - Pipelined/parallel converters - High speed ADC design, High speed DAC design and Mixed signal design for radar application - ADC and DAC modules used for LIGO.

PLL

SENSOR INTERFACING
Sensors, Sensor Types, Amplifier Design, Interfacing of Temperature, Pressure, Displacement Transducer in Embedded System Environment

LCD AND INFRA RED
LCD Fundamentals, Response Time, Temperature Effects, Connection Methods, Different types of LCD Panels, Static Waveforms, Infra Red Detection and Transmission

TIME-BASED MEASUREMENTS
Measuring Period versus Frequency, Mixing, Voltage-to-Frequency Converters, Clock Resolution and Range, Extending Accuracy with Limited Resolution

TEXT BOOKS:
1. Analog Interfacing to Embedded Microprocessors Real World Design, Stuart Ball.

REFERENCE BOOKS:
**CAD System Environment**

Familiarity with Unix/ Linux / Sun OS

**Basic Concept of Operating System:** Evolution of operating system, fundamental of operating system functions, multiprocessing, multiprogramming, time sharing systems and real time systems.

**Linux:** Brief History , Linux Distributions , Using the Emacs Editor , Using the vi Editor , Using the Pico Editor , Introduction to Users and Groups Essentials of Effective User, Group, and Password Management , Introduction to the Linux Kernel ,Using Kernel Modules ,Compiling the Linux Kernel ,Installing the Linux Kernel . File System , Disk Geometary

**UNIX:** Familiarity with different shells ,UNIX Utilities like tar, make, yacc, lex, lint, debugger etc.Programming Tools : Perl, tcl/ tk File formats .tgz, .tar, X-term environment

**SUN OS:** The Solaris Operating Environment, Specific Features, Solaris Web Start Wizards, DHCP, Web-based enterprise management, Solaris Management Console, role-based access control (RBAC), Sun Management Center, Solaris Volume Manager, Solaris Resource Manager, Solaris Bandwidth Manager, Extensive Linux Compatibility

**Windows NT,XP Environment**

Familiarity with PVM: creating a parallel virtual environment, initiating server and daemons, PVM library routines, XPVM
**Elective II**

**VLSI Testing and Design for Testability**

Physical defects and their modeling; stuck at faults; Bridging Faults; Fault collapsing.

Fault Simulation: Deductive, Parallel and Concurrent; Critical Path Tracing.

Test Generation for Combinational Circuits: D-Algorithm, Boolean Difference, PODEM, and ATPG.

Random, Exhaustive and Weighted Random Test Pattern Generations Aliasing and its effect on Fault coverage.

PLA Testing: cross-point Fault Model, Test Generation,

Memory testing: Permanent Intermittent and Pattern Sensitive Faults; Delay Faults and Hazards; Test Generation Techniques;

Test Generation for Sequential Circuits.

Scan Design. Scan path and LSSD, BILBO

Concept of Redundancy, spatial redundancy, Time redundancy

Recent trends in VLSI testing: Genetic Algorithms, Parallel Algorithms, Neural networks, nano scale testing

**Text books:**

1. VLSI Testing: digital and mixed analogue digital techniques Stanley L. Hurst
   Pub:Inspec/IEE ,1999
Low Power VLSI Design

Low power Basics
Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Device & Technology Impact on Low Power
Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Power estimation
Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems.

Low Power Design
Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network


Text:

References:
**CAD for VLSI**

Introduction to VLSI design methodologies and supporting CAD environment.


Simulation: Types of simulation, Behavioral simulator, logic simulator, functional simulator & Circuit simulator.


Testing ICs: Fault simulation, Aids for test generation and testing. Computational complexity issues: Big Oh and big omega terms.

Recent topics in CAD-VLSI: Array compilers, hardware software co-design, high-level synthesis tools and VHDL modeling.

**Books:**
1. Trimburger, ”Introduction to CAD for VLSI”, Kluwer Academic publisher, 2002
Algorithms for VLSI Design Automation

VLSI physical design automation and Fabrication
VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices

VLSI automation Algorithms:
Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing.

Floor planning & pin assignment: problem formulation, classification of floor planning algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design, chip planning, pin assignment, problem formulation, classification of pin assignment algorithms, General & channel pin assignment

Placement
Problem formulation, classification of placement algorithms, simulation base placement algorithms, recent trends in placement

Global Routing and Detailed routing: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, performance driven routing
Detailed routing problem formulation, classification of routing algorithms, introduction to single layer routing algorithms, two layer channel routing algorithms, greedy channel routing, switchbox routing algorithms.

Over the cell routing & via minimization: two layers over the cell routers, constrained & unconstrained via minimization

Compaction: problem formulation, classification of compaction algorithms, one-dimensional compaction, two dimension based compaction, hierarchical compaction

Text Books:

References